WHAT IS CLAIMED IS:

1. An apparatus comprising:

a memory subsystem;

a memory controller coupled to said memory subsystem and configured to control accesses to said memory subsystem; and

a temperature sensor positioned to detect a temperature associated with said memory subsystem;

wherein said memory controller is configured to selectively insert one or more idle clock cycles between a first memory access and a second memory access depending upon said sensed temperature.

2. The apparatus of claim 1, wherein in response to said sensed temperature being greater than a predetermined threshold, said memory controller is configured to insert said one or more idle clock cycles between said first memory access and said second memory access.

3. The apparatus of claim 2, wherein in response to said sensed temperature being greater than said predetermined threshold, said memory controller is configured to insert said one or more idle clock cycles between every $n^{th}$ and $n^{th}+1$ memory access.

4. The apparatus of claim 1, further comprising a service processor coupled to said memory controller and configured to receive a control signal from said temperature sensor.

5. The apparatus of claim 4, wherein in response to said control signal indicating that said sensed temperature is greater than a predetermined threshold, said service processor

is further configured to program said memory controller to insert said one or more idle clock cycles.

6. The apparatus of claim 5, wherein said memory controller is configured to insert said one or more idle cycles between each of a plurality of additional memory accesses.

7. The apparatus of claim 5, wherein said service processor is configured to change a rate at which idle cycles are inserted between a plurality of additional memory accesses depending upon said sensed temperature.

8. The apparatus of claim 7, wherein said rate is changed to a linear rate.

9. The apparatus of claim 7, wherein said rate is changed to an exponential rate.

10. The apparatus of claim 5, wherein said service processor is configured to change a number of idle cycles that are inserted between a plurality of additional memory accesses depending upon said sensed temperature.

11. A method comprising:

sensing a temperature associated with a memory subsystem; and

selectively inserting one or more idle clock cycles between a first memory access and a second memory access depending upon said sensed temperature.

12. The method of claim 11, wherein in response to said sensed temperature being greater than a predetermined threshold, inserting said one or more idle clock cycles between a plurality of memory accesses at a particular rate.

13. An apparatus comprising:

a memory subsystem;

a memory controller coupled to said memory subsystem and configured to control accesses to said memory subsystem; and

a sensor coupled to detect a power condition associated with said memory subsystem;

wherein said memory controller is configured to selectively insert one or more idle clock cycles between a first memory access and a second memory access depending upon said detected power condition.

14. The apparatus of claim 13, wherein said detected power condition is a current draw associated with said memory subsystem.

15. The apparatus of claim 14, wherein in response to said detected current draw being greater than a predetermined threshold, said memory controller is configured to insert said one or more idle clock cycles between every $n^{th}$ and $n^{th}+1$ memory access.

16. The apparatus of claim 14, further comprising a service processor coupled to said memory controller and configured to receive a control signal from said sensor.

17. The apparatus of claim 16, wherein in response to said control signal indicating that said detected current draw is greater than a predetermined threshold, said service processor is further configured to program said memory controller to insert said one or more idle clock cycles.

18. The apparatus of claim 17, wherein said memory controller is configured to insert said one or more idle cycles between each of a plurality of additional memory accesses.

19. The apparatus of claim 17, wherein said service processor is configured to change a rate at which idle cycles are inserted between a plurality of additional memory accesses depending upon said detected current draw.

20. A method comprising:

detecting a power condition associated with a memory subsystem; and

selectively inserting one or more idle clock cycles between a first memory access and a second memory access depending upon said detected power condition.

21. The method of claim 20, wherein said detected power condition is a current draw associated with said memory subsystem, wherein in response to said detected current draw being greater than a predetermined threshold, inserting said one or more idle clock cycles between a plurality of memory accesses at a particular rate.

22. A computer system comprising:

a processor;

a memory subsystem;

a memory controller coupled to said processor and said memory subsystem, wherein said memory controller is configured to control accesses to said memory subsystem by said processor;

a temperature sensor positioned to detect a temperature associated with said memory subsystem; and

a service processor coupled to said memory controller, wherein in response to said sensed temperature being greater than a predetermined threshold, said service processor is configured to program said memory controller to insert one or more idle clock cycles between a first memory access and a second memory access.

23. A computer system comprising:

a processor;

a memory subsystem;

a memory controller coupled to said processor and said memory subsystem, wherein said memory controller is configured to control accesses to said memory subsystem by said processor;

a sensor coupled to detect a current draw associated with said memory subsystem; and

a service processor coupled to said memory controller, wherein in response to said detected current draw being greater than a predetermined threshold, said service processor is configured to program said memory controller to insert one or more idle clock cycles between a first memory access and a second memory access.